

What is claimed is:

- 1 1. A method of forming a gate electrode, comprising:
 - 2 forming a first layer of a first material having a first work function on a
 - 3 substrate;
 - 4 forming a second layer of a second material over the first layer, the
 - 5 second material having a second work function; and
 - 6 removing a portion of the first and second layers;
 - 7 wherein a stack formed by the first and second layers has a work function
 - 8 that is between the first work function and the second work function.
- 1 2. The method Claim 1, wherein the substrate is a silicon wafer with an
 - 2 insulating layer formed thereon.
- 1 3. The method of Claim 2, wherein the insulating layer comprises an oxide of
 - 2 silicon.
- 1 4. The method of Claim 2, wherein the second layer is substantially thicker
 - 2 than the first layer.
- 1 5. The method of Claim 2, further comprising providing an optimal channel
 - 2 doping for a predetermined relationship between an on current, I_{on} , and an off
 - 3 current, I_{off} .

1 6. An insulated gate FET, comprising:
2 a gate dielectric layer disposed on a substrate;
3 a gate electrode disposed over the gate dielectric; and
4 a pair of source/drain regions disposed in the substrate along laterally
5 opposed sidewalls of the gate electrode;
6 wherein the gate electrode comprises a first material superjacent the gate
7 dielectric, a second material superjacent the first the first material, the first
8 material being a diffusion barrier with respect to the second material, and the
9 thickness of the first material is such that the work function of the gate electrode
10 is the work function of the second material.

1 7. The insulated gate FET of Claim 6, wherein the first material comprises
2 TiN, and the second material comprises Al.

1 8. The insulated gate FET of Claim 6, wherein the first material comprises
2 TiN, and the second material comprises Pd.

1 9. The insulated gate FET of Claim 6, wherein the first material comprises
2 TaN, and the second material comprises Pd.

1 10. A method of tuning the work function of a gate electrode, comprising:
2 forming a layer of a first conductive material superjacent a gate dielectric;
3 and

4 forming a layer of a second conductive material superjacent the first
5 conductive material;
6 wherein the thickness of the first conductive material is greater than a first
7 critical thickness and less than a second critical thickness.

1 11. The method of Claim 10, wherein the first conductive material comprises a
2 material selected from the group consisting of TiN, and TaN.

1 12. The method of Claim 10, wherein the second conductive material
2 comprises a material selected from the group consisting Al, Ti, Ta, Ni, Pd, and
3 Pt.

1 13. The method of Claim 10, wherein the first conductive material comprises
2 TiN, the second material comprises Al, the first critical thickness is approximately
3 20 angstroms and the second critical thickness is approximately 100 angstroms.

1 14. A method of making a field effect transistor, comprising:
2 forming a gate dielectric disposed on a semiconductor, a gate electrode
3 comprising a first material disposed over the gate dielectric, and a pair of
4 source/drain regions substantially disposed in the semiconductor and aligned to
5 laterally opposed sidewalls of the gate electrode; and
6 forming a work function modulation layer comprising a second material
7 disposed intermediate the gate dielectric and the gate electrode, wherein the

8 thickness of the work function modulation layer is such that the work function of
9 the gate electrode is different than the work function of the first material and
10 different from the work function of the second material.

1 15. The method of Claim 14, wherein the work function modulation layer acts
2 as a diffusion barrier to substantially preclude diffusion of the first material into
3 the gate dielectric.

1 16. The method of Claim 14, wherein the work function modulation layer is
2 titanium nitride.

1 17. The method of Claim 15, wherein the work function modulation layer is
2 tantalum nitride.

1 18. An integrated circuit, comprising:
2 an n-channel FET having a gate electrode comprising a first TiN layer
3 superjacent a first gate dielectric and an Al layer superjacent the first TiN layer;
4 and
5 a p-channel FET having a gate electrode comprising a second TiN layer
6 superjacent a second gate dielectric and a Pd layer superjacent the second TiN
7 layer.

1 19. The integrated circuit of Claim 18, wherein the first TiN layer is between
2 approximately one atomic monolayer and 100 angstroms thick; and the second
3 TiN layer is between one atomic monolayer and 100 angstroms thick.

1 20. The integrated circuit of Claim 18, wherein the first TiN is approximately
2 10 angstroms thick and the second TiN is approximately 20 angstroms thick.

1 21. An integrated circuit, comprising:
2 an n-channel FET having a gate electrode comprising a TiN layer
3 superjacent a first gate dielectric and an Al layer superjacent the TiN layer; and
4 a p-channel FET having a gate electrode comprising a TaN layer
5 superjacent a second gate dielectric and a Pd layer superjacent the TaN layer.

1 22. The integrated circuit of Claim 21, wherein the TiN layer is between
2 approximately one atomic monolayer and 100 angstroms thick; and the TaN
3 layer is between one atomic monolayer and 100 angstroms thick.

1 23. The integrated circuit of Claim 21, wherein the TiN is approximately 20
2 angstroms thick.

1 24. The integrated circuit of Claim 23, wherein the TiN is an Al diffusion
2 barrier, and the TaN is a Pd diffusion barrier.

1 25. An integrated circuit, comprising:
2 a first FET of a first conductivity type, the first FET having a first work
3 function modulation layer; and
4 a second FET of the first conductivity type; the second FET having a
5 second work function modulation layer;
6 wherein the first and second work function modulation layers comprise the
7 same material, and the thickness of the first work function modulation layer is
8 different than the thickness of the second work function modulation layer.

1 26. The integrated circuit of Claim 25, wherein the first and second FETs have
2 substantially identical channel doping profiles and the first and second FETs
3 have different threshold voltages.